FLORIDA ATLANTIC UNIVERSITY

NEW COURSE PROPOSAL
Graduate Programs

Department Computer & Elec. Eng. and Computer Sci

College College of Engineering and Computer Science

*(To obtain a course number, contact **erudolph@fau.edu**)*

UGPC Approval _____
UFS Approval _____
SCNS Submittal _____
Confirmed _____
Banner Posted _____
Catalog _____

Prefix EEE **Number** 5324	*(L = Lab Course; C = Combined Lecture/Lab; add if appropriate)* **Lab Code**	**Course Title** Silicon Integrated Circuit Fabrication
Credits *(Review Provost Memorandum)* 3 **Effective Date** *(TERM & YEAR)* Fall 2017	**Grading** *(Select One Option)* **Regular** (●) **Sat/UnSat** ( )	**Course Description** *(Syllabus must be attached; see Guidelines)* This course provides an introduction to the basic steps and processes of fabricating integrated circuit semiconductor devices. Standard Si IC fabrication processes (oxidation, diffusion, etching, photolithography, ion implantation, chemical mechanical polishing, chemical vapor deposition, front and back end integration) will also be covered. Concepts and processes related to BioMEMS and microfluidics will also be explained.

Prerequisites	**Corequisites**	**Registration Controls** *(Major, College, Level)*
Graduate Status Level OR Circuits I (EEL 3111) and Electronics I (EEE 3300).	N/A	Graduates in College of Eng. & Comp. Sci., and Seniors

Prerequisites, Corequisites and Registration Controls are enforced for all sections of course

Minimum qualifications needed to teach course: Member of the FAU graduate faculty and has a terminal degree in the subject area (or a closely related field.)	**List textbook information in syllabus or here** Silicon Processing for the VLSI Era, Volume 1 - Process Technology, Second Edition, S. Wolf and R. N. Tauber, ISBN: 0-9616721-6-1, 1999
Faculty Contact/Email/Phone Waseem Asghar wasghar@fau.edu	**List/Attach comments from departments affected by new course** N/A

Approved by	***Date***
Department Chair	02/03/17
College Curriculum Chair	2/6/17
College Dean	2/6/17
UGPC Chair	
Graduate College Dean	
UFS President	
Provost	

Email this form and syllabus to UGPC@fau.edu one week before the UGPC meeting.

Department of Computer & Electrical Engineering
and Computer Science
Florida Atlantic University
Course Syllabus

1. Course title/number, number of credit hours	
Silicon Integrated Circuit Fabrication EEE 5324	# of credit hours = 3
2. Course prerequisites, corequisites, and where the course fits in the program of study	
Prerequisites: Graduate Status Level OR Circuits I (EEL 3111) and Electronics I (EEE 3300).	
3. Course logistics	
Term: Fall 2017 Location: TBD	
4. Instructor contact information	
Instructor's name *Office address* *Office Hours* *Contact telephone number* *Email address*	Waseem Asghar, PhD Bldg. EE 96/ Room 435 TBD 561-297-2800 wasghar@fau.edu
5. TA contact information	
TA's name *Office address* *Office Hours* *Contact telephone number* *Email address*	TBD
6. Course description	
This course provides an introduction to the basic steps and processes of fabricating integrated circuit semiconductor devices. Standard Si IC fabrication processes (oxidation, diffusion, etching, photolithography, ion implantation, chemical mechanical polishing, chemical vapor deposition, front and back end integration) will also be covered. Concepts and processes related to BioMEMS and microfluidics will also be explained.	
7. Course objectives/student learning outcomes/program outcomes	
Course objectives	To introduce the students to the concepts of silicon integrated circuit fabrication processes and modules.
8. Course evaluation method	
5 Homework assignments (4% each) : 20% Term paper: 20% Midterm exam: 20% Final exam: 40%	For term paper, students will be divided into group of 2-3 students. Each group will propose an interesting topic related to latest key advances in the field of Silicon Integrated Circuit Fabrication. Each group will present their proposal topic in class and also submit a comprehensive report on the

	proposed topic.

9. Course grading scale

Grading Scale:
90 and above: "A", 87-89: "A-", 83-86: "B+", 80-82: "B", 77-79 : "B-", 73-76: "C+", 70-72: "C", 67-69: "C-", 63-66: "D+", 60-62: "D", 51-59: "D-", 50 and below: "F."

10. Policy on makeup tests, late work, and incompletes

Students are strongly suggested to inform the instructor in advance in the case of emergency (if possible). Makeup exams are given only if there is solid evidence of a medical or otherwise serious emergency that prevents the student of participating in the exam.

Students must turn in homework, assignment and projects on time. Students may lose 25% (after 1 day) and 50% of marks (after 2 days) if they turn in late. Submissions may not accepted after 2nd day of due date.

11. Special course requirements

12. Classroom etiquette policy

University policy requires that in order to enhance and maintain a productive atmosphere for education, personal communication devices, such as cellular phones and laptops, are to be disabled in class sessions.

13. Disability policy statement

In compliance with the Americans with Disabilities Act Amendments Act (ADAAA), students who require reasonable accommodations due to a disability to properly execute coursework must register with Student Accessibility Services (SAS)—in Boca Raton, SU 133 (561-297-3880); in Davie, LA 131 (954-236-1222); or in Jupiter, SR 111F (561-799-8585) —and follow all SAS procedures.

14. Honor code policy

Students at Florida Atlantic University are expected to maintain the highest ethical standards. Academic dishonesty is considered a serious breach of these ethical standards, because it interferes with the university mission to provide a high quality education in which no student enjoys unfair advantage over any other. Academic dishonesty is also destructive of the university community, which is grounded in a system of mutual trust and place high value on personal integrity and individual responsibility. Harsh penalties are associated with academic dishonesty. See University Regulation 4.001 at www.fau.edu/regulations/chapter4/4.001_Code_of_Academic_Integrity.pdf

15. Required texts/reading

Silicon Processing for the VLSI Era, Volume 1 - Process Technology, **Second Edition**,
S. Wolf and R. N. Tauber, ISBN: 0-9616721-6-1, 1999

16. Supplementary/recommended readings

Research papers will be given at the end of lectures to read and understand.

1. Lee et al. "Ge GAA FETs and TMD FinFETs for the Applications Beyond Si—A Review", IEEE Journal of the Electron Devices Society (Volume: 4, Issue: 5, Sept. 2016).
2. Tans et al. "Room-temperature transistor based on a single carbon nanotube", Nature 393, 49-52 (7 May 1998)
3. Das et al. "Mechanisms of material removal and mass transport in focused ion beam nanopore formation", Journal of Applied Physics , Volume 117, Issue 8, 2015
4. Feynman, "There's plenty of room at the bottom", the annual meeting of the American Physical Society (APS) at the California Institute of Technology, 1959
5. Kim et al., "Silicon-Based BioFETs with 3-D Nanostructure: Easy integration, precise control of nanostructure, and a low device-to-device variation", IEEE Nanotechnology Magazine (Volume: 10, Issue: 3, Sept. 2016)
6. Mariana et al., "An Inkjet-Printed Field-Effect Transistor for Label-Free Biosensing", Advanced Functional Materials, 2014
7. Vacic et al., "Calibration methods for silicon nanowire BioFETs", International Conference on Microelectronic Test Structures (ICMTS), 2014
8. Ye at al., "Atomic layer deposition of ZrO_2 as gate dielectrics for AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors on silicon", Applied Physics Letters, Volume 103, Issue 14, 2014

17. Course topical outline, including dates for exams/quizzes, papers, completion of reading

Weekly Schedule	Topics
Week 01	IC Process Overview & Wafer Fabrication: Historical perspective –a sampling of key inventions and discoveries, Design-to-package workflow Fab process types, crystal structure basics, physical properties
Week 02	Crystal Defects: Monovacancy, Divacancy, Microvoids, Voids, Antisites, Interstitials, Dislocation, Stacking fault, Grain Boundaries, Precipitates. Wafer Fabrication: Czochralski (CZ), Float Zone (FZ), Molecular Beam Epitaxy
Week 03	Thermal Oxidation: Oxidation kinetics (general solution, Parabolic and linear growth and empirical modifications to the growth rate of SiO_2 and its kinetics), Thermal Nitridation Factors in oxidation, Applications of oxide and nitride layers in IC fabrication, SiO_2/Si interface, charge traps and impurities redistribution at the interface, Oxidation systems, Measurement techniques **HW-1**
Week 04	Diffusion: Fick's first and second law and their solutions, Mechanism of diffusion, Profile and Junction Depth and techniques of their determination Effect of electric field on diffusion process Impurity diffusion in IC fabrication (Boron, Phosphorus, Ar). Diffusion Systems [equipment, sources (gas, liquid, solid)] Measurement techniques.

	HW-2
Week 05	Lithography 1 - Photoresists (positive and negative) Resist chemistry (Photo sensitive and base) Physical properties (Sensitivity, Photo Speed, Resolution, etc.) Resists and Process: Photolithography steps (Coat, Soft bake, Patterning and Exposure, Post Exposure Bake, Develop, Inspection) Coat and Coaters (Thickness control, uniformity, etc.), Soft Bake and its effects on the film properties and consequent steps
Week 06	Lithography 2: Patterning and exposure, Criteria, limits, resist dependency, equipment, alignment, etc.) Bosung Curves, Focus-exposure matrix, Post Exposure Bake, and its effects on the pattern, Develop (batch, spray, and puddle). **HW-3**
Week 07	Developer chemistry, development time, Critical Dimensions (CD) and Inspection (pattern integrity, notching, bridging, etc.) **Midterm Exam**
Week 08	Etch and Cleans: Introduction to dry etch, Etch output parameters, Process monitoring (OES and EPD), Etch Equipment Cleans: Intro to contamination types, sources, and impact, Wafer cleaning, Particle removal, Defect detection For term paper proposal, students will be divided into group of 2-3 students. Each group will propose an interesting topic related to latest key advances in the filed of Silicon Integrated Circuit Fabrication. Each group will present their proposal topic in class and also submit a comprehensive report on the proposed topic. **Term Paper Proposal**
Week 09	Chemical Vapor Deposition: Introduction to Chemical Vapor Deposition (CVD), Basics, Grove's simplified growth model, Gas flow CVD Systems Systems, Reactors, MFCs, PECVD, Example films deposited by CVD: Polysilicon, SiO_2, Silicon Nitride, Tungsten **HW-4**
Week 10	Epitaxy: Epitaxy: Intro and Applications, Growth, Defects, Low Temperature Growth Selective Epitaxy, Strained Silicon, Equipment, Characterization
Week 11	Physical Vapor Deposition: Thermal Evaporation, E-beam Evaporation, SOI Wafers Sputtering Process: Sputtering deposition and Equipment, Applications of Sputtering, glow discharge, RF sputter, magnetron sputter, mechanism,

	deposition rate, advantages and disadvantages, etc.), Contacts and Vias, Morphology and Step Coverage, Aspect Ratio **HW-5**
Week 12	Ion Implantation: Dose, Beam Current, Range and Projected Range Projected and Lateral Straggle, Ion Stopping (nuclear and electronic energy loss mechanism), Implantation in amorphous and single crystal (channeling effect) Ion implantation damage, Electrical activation and implantation damage recovery (Annealing and RTP), Ion Implantation equipment, Masking layers, Shallow Junction, Measurement techniques
Week 13	Back-End Integration: Introduction & Conventional Flow, Propagation Delay, Choice of Materials Metal Deposition and Via Filling, Aluminum, Tungsten, Copper, Low-k Dielectrics, Damascene Integration
Week 14	Planarization and Passivation: BPSG Reflow, Etch Back, Deposition Etch Cycles, Spin on Glass, Choice of Deposition Chemical Mechanical Polishing: Intro to CMP, Local and Global Planarization, Dummy Features, CMP Removal Rates, Slurry Types, Pad Types, Slurry, CMP Defects.
Week 15	Front-End Integration: Introduction and History, 0.5μm to 1.2μm Process Flow (circa 1990), Wells and Channel stop, LOCOS isolation, Vt adjust and Gate formation, Source/Drains, PMD and Contacts Deep-sub Micron (<0.25 μm) Process Flow (circa 2000), Shallow Trench, Isolation, Retrograde Wells and Vt adjust, Gate formation, Source/Drains with extensions (tips), Salicide, PMD and Contacts **Term Paper Presentation and Report Submission**
	Final Exam