



FLORIDA  
ATLANTIC  
UNIVERSITY

## NEW COURSE PROPOSAL Graduate Programs

**Department** Computer & Elec. Eng. and Computer Sci

**College** College of Engineering and Computer Science  
(To obtain a course number, contact [erudolph@fau.edu](mailto:erudolph@fau.edu))

UGPC Approval \_\_\_\_\_

UFS Approval \_\_\_\_\_

SCNS Submittal \_\_\_\_\_

Confirmed \_\_\_\_\_

Banner Posted \_\_\_\_\_

Catalog \_\_\_\_\_

**Prefix** EEE

(L = Lab Course; C =  
Combined Lecture/Lab;  
add if appropriate)

**Course Title**

Silicon Integrated Circuit Fabrication

**Number** 5324

**Lab  
Code**

**Credits** (Review  
*Provost Memorandum*)

3

**Grading**  
(Select One Option)

Regular

Sat/UnSat

**Course Description** (Syllabus must be attached; see [Guidelines](#))

This course provides an introduction to the basic steps and processes of fabricating integrated circuit semiconductor devices. Standard fabrication processes (oxidation, diffusion, etching, lithography, ion implantation, chemical vapor deposition, front and back end integration) will be covered.

**Effective Date**  
(TERM & YEAR)

Fall 2017

**Prerequisites**

Graduate Status Level OR  
Circuits I (EEL 3111) and Electronics I  
(EEE 3300).

**Corequisites**

N/A

**Registration Controls** (Major,  
College, Level)

Graduates, Seniors (College of  
Engineering)

*Prerequisites, Corequisites and Registration Controls are enforced for all sections of course*

**Minimum qualifications needed to teach  
course:**

Member of the FAU graduate faculty  
and has a terminal degree in the  
subject area (or a closely related field.)

**List textbook information in syllabus or here**

Silicon Processing for the VLSI Era, Volume 1 - Process  
Technology, Second Edition,  
S. Wolf and R. N. Tauber, ISBN: 0-9616721-6-1, 1999

**Faculty Contact/Email/Phone**

Waseem Asghar  
[wasghar@fau.edu](mailto:wasghar@fau.edu)

**List/Attach comments from departments affected by new course**

College of Science

**Approved by**

Department Chair

*[Signature]*

College Curriculum Chair

*[Signature]*

College Dean

*[Signature]*

UGPC Chair

Wm R McDaniel P.R.P.

Graduate College Dean

*[Signature]*

UFS President

Provost

**Date**

02/03/17

2/6/17

2/6/17

3-1-2017

3-5-17

Email this form and syllabus to [UGPC@fau.edu](mailto:UGPC@fau.edu) one week before the UGPC meeting.

**Department of Computer & Electrical Engineering  
and Computer Science  
Florida Atlantic University  
Course Syllabus**

<b>1. Course title/number, number of credit hours</b>	
Silicon Integrated Circuit Fabrication EEE 5324	# of credit hours = 3
<b>2. Course prerequisites, corequisites, and where the course fits in the program of study</b>	
Prerequisites: Graduate Status Level OR Circuits I (EEL 3111) and Electronics I (EEE 3300).	
<b>3. Course logistics</b>	
Term: Fall 2017 Location: TBD	
<b>4. Instructor contact information</b>	
<i>Instructor's name</i>	Waseem Asghar, PhD
<i>Office address</i>	Bldg. EE 96/ Room 435
<i>Office Hours</i>	TBD
<i>Contact telephone number</i>	561-297-2800
<i>Email address</i>	<a href="mailto:wasghar@fau.edu">wasghar@fau.edu</a>
<b>5. TA contact information</b>	
<i>TA's name</i>	TBD
<i>Office address</i>	
<i>Office Hours</i>	
<i>Contact telephone number</i>	
<i>Email address</i>	
<b>6. Course description</b>	
This course provides an introduction to the basic steps and processes of fabricating integrated circuit semiconductor devices. Standard fabrication processes (oxidation, diffusion, etching, lithography, ion implantation, chemical vapor deposition, front and back end integration) will be covered. Concepts and processes related to BioMEMS and microfluidics will also be explained.	
<b>7. Course objectives/student learning outcomes/program outcomes</b>	
<i>Course objectives</i>	To introduce the students to the concepts of silicon integrated circuit fabrication processes and modules.
<b>8. Course evaluation method</b>	
5 Homework assignments (4% each) : 20%	For term paper, students will be divided into group of 2-3 students. Each group will propose an interesting topic related to latest key advances in the field of Silicon Integrated Circuit Fabrication. Each group will present their proposal topic in class and also submit a comprehensive report on the proposed topic.
Term paper: 20%	
Midterm exam: 20%	
Final exam: 40%	

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<b>9. Course grading scale</b>
Grading Scale: 90 and above: "A", 87-89: "A-", 83-86: "B+", 80-82: "B", 77-79: "B-", 73-76: "C+", 70-72: "C", 67-69: "C-", 63-66: "D+", 60-62: "D", 51-59: "D-", 50 and below: "F."
<b>10. Policy on makeup tests, late work, and incompletes</b>
Students are strongly suggested to inform the instructor in advance in the case of emergency (if possible). Makeup exams are given only if there is solid evidence of a medical or otherwise serious emergency that prevents the student of participating in the exam.  Students must turn in homework, assignment and projects on time. Students may lose 25% (after 1 day) and 50% of marks (after 2 days) if they turn in late. Submissions may not accepted after 2 <sup>nd</sup> day of due date.
<b>11. Special course requirements</b>
<b>12. Classroom etiquette policy</b>
University policy requires that in order to enhance and maintain a productive atmosphere for education, personal communication devices, such as cellular phones and laptops, are to be disabled in class sessions.
<b>13. Disability policy statement</b>
In compliance with the Americans with Disabilities Act Amendments Act (ADAAA), students who require reasonable accommodations due to a disability to properly execute coursework must register with Student Accessibility Services (SAS)—in Boca Raton, SU 133 (561-297-3880); in Davie, LA 131 (954-236-1222); or in Jupiter, SR 111F (561-799-8585)—and follow all SAS procedures.
<b>14. Honor code policy</b>
Students at Florida Atlantic University are expected to maintain the highest ethical standards. Academic dishonesty is considered a serious breach of these ethical standards, because it interferes with the university mission to provide a high quality education in which no student enjoys unfair advantage over any other. Academic dishonesty is also destructive of the university community, which is grounded in a system of mutual trust and place high value on personal integrity and individual responsibility. Harsh penalties are associated with academic dishonesty. See University Regulation 4.001 at <a href="http://www.fau.edu/regulations/chapter4/4.001_Code_of_Academic_Integrity.pdf">www.fau.edu/regulations/chapter4/4.001_Code_of_Academic_Integrity.pdf</a>
<b>15. Required texts/reading</b>
Silicon Processing for the VLSI Era, Volume 1 - Process Technology, <b>Second Edition</b> , S. Wolf and R. N. Tauber, ISBN: 0-9616721-6-1, 1999
<b>16. Supplementary/recommended readings</b>
Research papers will be given at the end of lectures to read and understand. 1. Lee et al. "Ge GAA FETs and TMD FinFETs for the Applications Beyond Si—A Review", IEEE

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- Journal of the Electron Devices Society ( Volume: 4, Issue: 5, Sept. 2016 ).
2. Tans et al. "Room-temperature transistor based on a single carbon nanotube", Nature 393, 49-52 (7 May 1998)
  3. Das et al. "Mechanisms of material removal and mass transport in focused ion beam nanopore formation", Journal of Applied Physics , Volume 117, Issue 8, 2015
  4. Feynman, "There's plenty of room at the bottom", the annual meeting of the American Physical Society (APS) at the California Institute of Technology, 1959
  5. Kim et al., "Silicon-Based BioFETs with 3-D Nanostructure: Easy integration, precise control of nanostructure, and a low device-to-device variation", IEEE Nanotechnology Magazine ( Volume: 10, Issue: 3, Sept. 2016 )
  6. Mariana et al., "An Inkjet-Printed Field-Effect Transistor for Label-Free Biosensing", Advanced Functional Materials, 2014
  7. Vacic et al., "Calibration methods for silicon nanowire BioFETs", International Conference on Microelectronic Test Structures (ICMTS), 2014
  8. Ye at al., "Atomic layer deposition of ZrO<sub>2</sub> as gate dielectrics for AlGaIn/GaN metal-insulator-semiconductor high electron mobility transistors on silicon", Applied Physics Letters, Volume 103, Issue 14, 2014

**17. Course topical outline, including dates for exams/quizzes, papers, completion of reading**

Weekly Schedule	Topics
Week 01	IC Process Overview & Wafer Fabrication: Historical perspective –a sampling of key inventions and discoveries, Design-to-package workflow  Fab process types, crystal structure basics, physical properties
Week 02	Crystal Defects: Monovacancy, Divacancy, Microvoids, Voids, Antisites, Interstitials, Dislocation, Stacking fault, Grain Boundaries, Precipitates.  Wafer Fabrication: Czochralski (CZ), Float Zone (FZ), Molecular Beam Epitaxy
Week 03	Thermal Oxidation: Oxidation kinetics (general solution, Parabolic and linear growth and empirical modifications to the growth rate of SiO <sub>2</sub> and its kinetics), Thermal Nitridation  Factors in oxidation, Applications of oxide and nitride layers in IC fabrication, SiO <sub>2</sub> /Si interface, charge traps and impurities redistribution at the interface, Oxidation systems, Measurement techniques  <b>HW-1</b>
Week 04	Diffusion: Fick's first and second law and their solutions, Mechanism of diffusion, Profile and Junction Depth and techniques of their determination Effect of electric field on diffusion process  Impurity diffusion in IC fabrication (Boron, Phosphorus, Ar). Diffusion Systems [equipment, sources (gas, liquid, solid)] Measurement techniques.  <b>HW-2</b>

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Week 05	<p>Lithography 1 - Photoresists (positive and negative) Resist chemistry (Photo sensitive and base) Physical properties (Sensitivity, Photo Speed, Resolution, etc.)</p> <p>Resists and Process: Photolithography steps (Coat, Soft bake, Patterning and Exposure, Post Exposure Bake, Develop, Inspection) Coat and Coaters (Thickness control, uniformity, etc.), Soft Bake and its effects on the film properties and consequent steps</p>
Week 06	<p>Lithography 2: Patterning and exposure, Criteria, limits, resist dependency, equipment, alignment, etc.) Bosung Curves,</p> <p>Focus-exposure matrix, Post Exposure Bake, and its effects on the pattern, Develop (batch, spray, and puddle).</p> <p><b>HW-3</b></p>
Week 07	<p>Developer chemistry, development time, Critical Dimensions (CD) and Inspection (pattern integrity, notching, bridging, etc.)</p> <p><b>Midterm Exam</b></p>
Week 08	<p>Etch and Cleans: Introduction to dry etch, Etch output parameters, Process monitoring (OES and EPD), Etch Equipment</p> <p>Cleans: Intro to contamination types, sources, and impact, Wafer cleaning, Particle removal, Defect detection</p> <p>For term paper proposal, students will be divided into group of 2-3 students. Each group will propose an interesting topic related to latest key advances in the field of Silicon Integrated Circuit Fabrication. Each group will present their proposal topic in class and also submit a comprehensive report on the proposed topic.</p> <p><b>Term Paper Proposal</b></p>
Week 09	<p>Chemical Vapor Deposition: Introduction to Chemical Vapor Deposition (CVD), Basics, Grove's simplified growth model, Gas flow</p> <p>CVD Systems Systems, Reactors, MFCs, PECVD, Example films deposited by CVD: Polysilicon, SiO<sub>2</sub>, Silicon Nitride, Tungsten</p> <p><b>HW-4</b></p>
Week 10	<p>Epitaxy: Epitaxy: Intro and Applications, Growth, Defects, Low Temperature Growth</p> <p>Selective Epitaxy, Strained Silicon, Equipment, Characterization</p>
Week 11	<p>Physical Vapor Deposition: Thermal Evaporation, E-beam Evaporation, SOI Wafers</p> <p>Sputtering Process: Sputtering deposition and Equipment, Applications of Sputtering, glow discharge, RF sputter, magnetron sputter, mechanism, deposition rate, advantages and disadvantages, etc.), Contacts and Vias, Morphology and Step Coverage, Aspect Ratio</p>

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	<b>HW-5</b>
Week 12	<p>Ion Implantation: Dose, Beam Current, Range and Projected Range Projected and Lateral Straggle, Ion Stopping (nuclear and electronic energy loss mechanism), Implantation in amorphous and single crystal (channeling effect)</p> <p>Ion implantation damage, Electrical activation and implantation damage recovery (Annealing and RTP), Ion Implantation equipment, Masking layers, Shallow Junction, Measurement techniques</p>
Week 13	<p>Back-End Integration: Introduction &amp; Conventional Flow, Propagation Delay, Choice of Materials</p> <p>Metal Deposition and Via Filling, Aluminum, Tungsten, Copper, Low-k Dielectrics, Damascene Integration</p>
Week 14	<p>Planarization and Passivation: BPSG Reflow, Etch Back, Deposition Etch Cycles, Spin on Glass, Choice of Deposition</p> <p>Chemical Mechanical Polishing: Intro to CMP, Local and Global Planarization, Dummy Features, CMP Removal Rates, Slurry Types, Pad Types, Slurry, CMP Defects.</p>
Week 15	<p>Front-End Integration: Introduction and History, 0.5<math>\mu</math>m to 1.2<math>\mu</math>m Process Flow (circa 1990), Wells and Channel stop, LOCOS isolation, Vt adjust and Gate formation, Source/Drains, PMD and Contacts</p> <p>Deep-sub Micron (&lt;0.25 <math>\mu</math>m) Process Flow (circa 2000), Shallow Trench, Isolation, Retrograde Wells and Vt adjust, Gate formation, Source/Drains with extensions (tips), Salicide, PMD and Contacts</p> <p><b>Term Paper Presentation and Report Submission</b></p>
	<b>Final Exam</b>

**From:** Charles Roberts  
**Sent:** Wednesday, February 15, 2017 9:10 AM  
**To:** Mihaela Cardei  
**Cc:** Waseem Asghar  
**Subject:** Re: Request of Approval - Silicon Integrated Circuit Fabrication

To: UGPC

Subject: EEE 5324 Integrated Circuit Fabrication

Date: 2/15/2017

The College of Science supports the College of Engineering in offering this course, NCP-EEE5324, and recommends approval by the Faculty Senate.

Charles Roberts  
Chair, Charles E. Schmidt College of Science Curriculum Committee  
Associate Dean of Graduate Studies  
Charles E. Schmidt College of Science

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**From:** Mihaela Cardei  
**Sent:** Wednesday, February 15, 2017 7:51:26 AM  
**To:** Charles Roberts  
**Cc:** Mihaela Cardei; Waseem Asghar  
**Subject:** Request of Approval - Silicon Integrated Circuit Fabrication

Dear Dr. Roberts,

The Department of Computer and Electrical Engineering and Computer Science (CEECS) is proposing a new course EEE 5324 Silicon Integrated Circuit Fabrication. Please find attached the course proposal.

This course was discussed in the UGPC yesterday on February 14th, and it was suggested to get a support letter from the College of Science.

Could you please review the proposal and email me your approval decision?

Thank you,  
Mihaela

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Mihaela Cardei, PhD  
Professor and Director Graduate Studies  
Computer & Electrical Engineering and Computer Science Department  
College of Engineering and Computer Science, FAU  
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